Code :RA07A40401 RA

III B.Tech I Semester (R07) Supplementary Examinations, May 2011
DIGITAL IC APPLICATIONS
(Electronics & Instrumentation Engineering)
(For students of RR,R05 regulation readmitted to III B.Tech I semester R07)
Time: 3 hours **Max Marks: 80**

Answer any FIVE questions
All questions carry equal marks

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1. (a) A single pull-up register to +5V is used to provide a constant logic 1 to 15 different 75LS00 inputs. What is the maximum value of this register? How much high state DC noise margin can be provided in this case?
   (b) Explain the concept of sinking and sourcing currents. How are they estimated for CMOS families?
2. (a) State the logic levels for:
      i. 5V CMOS family.
      ii. 3.3V LVTTL family.
      iii. 1.8 V CMOS family.
      iv. 2.5V CMOS family.
   (b) Why IC industry is moving forward lower power supply voltages?
3. (a) Explain the difference between VHDL program structure and other procedural language program structure.
   (b) i. What is package declaration? Give example.
      ii. Explain IF statement in VHDL with example.
4. Explain in detail about modeling styles in VHDL hardware in description language with suitable examples.
5. (a) Implement following multiple output function using 74LS138 and external gates.
   F_1 (A.B.C) $=\sum m(1457), F_2(A, B, C) = \Pi M(2, 3, 6, 7)$
   (b) Write a VHDL source code for 4 input priority encoder.
   (c) Write a VHDL source code for 4:1 multiplexer.
6. (a) Write a VHDL program for a dual-priority encoder can be written using a nested IF loop.
   (b) Write a VHDL program for simple floating point encoder.
7. (a) Design on 8-bit synchronous binary counter with serial enable control.
   (b) Write architecture for counting in excess-3 counter using VHDL.
8. (a) Realize the logic functions performed by 74X381 with ROM.
   (b) Design on 8 X 4 diode ROM using 74X138 for the following data starting from the first location 1, 4, 9, B, A, O, F, C.
   (c) What is decoding?

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